

FORM PTO - 1449 *

INFORMATION DISCLOSURE STATEMENT

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ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>SP</i>	A217	2003/0227057	12/01/2003	Lochtefeld et al.			10/04/2002
	A218	2003/0230778 A1	12/18/2003	Park et al.			01/30/2003
	A219	2003/0232467 A1	12/18/2003	Anderson et al.			05/29/2003
	A220	2004/0005740	01/01/2004	Lochtefeld et al.			06/06/2003
	A221	2004/0007724 A1	01/15/2004	Murthy et al.			07/12/2002
	A222	2004/0009649 A1	01/15/2004	Kub et al.			05/20/2003
	A223	2004/0012037 A1	01/22/2004	Venkatesan et al.			07/18/2002
	A224	2004/0012075 A1	01/22/2004	Bedell et al.			07/16/2002
	A225	2004/0014304 A1	01/22/2004	Bhattacharyya			07/18/2002
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	A227	2004/0031979	02/19/2004	Lochtefeld et al.			06/06/2003
	A228	2004/0031990 A1	02/19/2004	Jin et al.			08/16/2002
	A229	2004/0041174 A1	03/04/2004	Okihara			03/21/2003
	A230	2004/0041210 A1	03/04/2004	Mouli			09/02/2003
	A231	2004/0048091 A1	03/11/2004	Sato et al.			09/04/2003
	A232	2004/0048454 A1	03/11/2004	Sakaguchi			09/04/2003
	A233	2004/0051140 A1	03/18/2004	Bhattacharyya			09/12/2002
	A234	2004/0053477 A1	03/18/2004	Ghyselen et al.			07/09/2003

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
<i>SP</i>	B1	41 01 167	07/23/1992	DE				No	No
	B2	0 514 018	11/19/1992	EP				No	Yes
	B3	0 587 520	03/16/1994	EP				No	Yes
	B4	0 683 522	11/22/1995	EP				No	Yes
	B5	0 828 296	03/11/1998	EP				No	Yes
	B6	0 829 908	03/18/1998	EP				No	Yes
	B7	0 838 858	04/29/1998	EP				No	No

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* : Pages 9 - 17 only.

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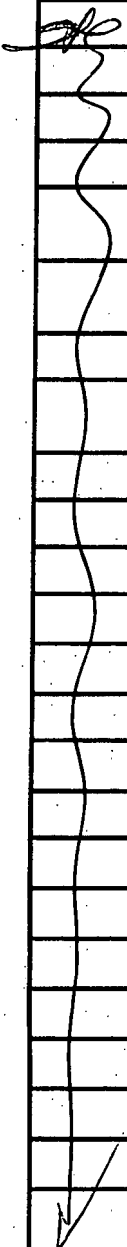
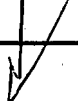
APPLICANTS: Cheng *et al.*

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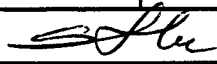
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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLAS S	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B8	1 020 900	07/19/2000	EP				No	Yes
	B9	1 174 928	01/23/2002	EP				No	Yes
	B10	2 342 777	04/19/2000	GB				Yes	Yes
	B11	4-307974	10/30/1992	JP				No	No
	B12	5-166724	07/03/1993	JP				No	Abstract Only
	B13	6-177046	06/24/1994	JP				No	Abstract Only
	B14	7-106446	04/21/1995	JP				No	No
	B15	7-240372	09/12/1995	JP				No	Abstract Only
	B16	10-270685	10/09/1998	JP				No	Yes
	B17	11-233744	08/27/1999	JP				No	No
	B18	2000-021783	01/21/2000	JP				No	Yes
	B19	2000-31491	01/28/2000	JP				No	No
	B20	2001319935	05/11/2000	JP				Yes	Yes
	B21	2002-076334	03/15/2002	JP				No	Yes
	B22	2002-164520	06/07/2002	JP				No	Yes
	B23	2002-289533	10/04/2002	JP				No	Yes
	B24	WO 98/59365	12/30/1998	PCT				No	Yes
	B25	WO 99/53539	10/21/1999	PCT				No	Yes
	B26	WO 00/48239	08/17/2000	PCT				No	Yes
	B27	WO 01/54202	07/26/2001	PCT				No	Yes
	B28	WO 01/99169A2	12/27/2001	PCT				No	Yes
	B29	WO 02/15244 A2	02/21/2002	PCT				No	Yes
	B30	WO 02/27783 A1	04/04/2002	PCT				No	Yes
	B31	WO 02/071495A1	09/12/2002	PCT				No	Yes

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<i>SL</i>	B32	WO 02/082514 A1	10/17/2002	PCT				No	Yes
	B33	WO 00/54338	09/14/2000	WO				No	Yes
	B34	WO 01/022482	03/29/2001	WO				No	Yes
	B35	WO 01/93338	12/06/2001	WO				No	Yes
	B36	WO 02/13262	02/14/2002	WO				No	Yes
	B37	WO 02/47168	06/13/2002	WO				No	Yes
	B38	WO 02/071488	09/12/2002	WO				No	Yes
	B39	WO 02/071491	09/12/2002	WO				No	Yes
	B40	WO 04/006311 A2	01/15/2004	WO			07/09/2003		YES
	B41	WO 04/006326 A1	01/15/2004	WO			07/09/2003		YES
	B42	WO 04/006327 A2	01/15/2004	WO			07/09/2003		YES
	B43	WO 04/019403 A2	03/04/2004	WO			08/26/2003		YES
<i>✓</i>	B44	WO 04/019404 A2	03/04/2004	WO			08/26/2003		YES

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
<i>SL</i>	C1	"2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," IBM Technical Disclosure Bulletin, Vol. 35, No. 4B (September 1992) pp. 136-140.
	C2	Armstrong et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEDM Technical Digest</u> (1995) pp. 761-764.
	C3	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices", Ph.D Thesis, Massachusetts Institute of Technology (1999) pp. 1-154.
	C4	Augusto et al., "Proposal for a New Process Flow for the Fabrication of Silicon-Based Complementary MOD-MOSFETs without Ion Implantation," <u>Thin Solid Films</u> , Vol. 294, No. 1-2 (1997) pp. 254-258.
<i>✓</i>	C5	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," <u>Modern Physics Letters B</u> (2001) (abstract).

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| C6 | Borenstein et al., "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," <u>Proceedings of the 1999 12th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)</u> (January 17-21, 1999) pp. 205-210. |
| C7 | Bouillon et al., "Search for the optimal channel architecture for 0.18/0.12 μ m bulk CMOS Experimental study," <u>IEEE</u> (1996) pp. 21.2.1-21.2.4. |
| C8 | Bruel et al., "©SMART CUT: A Promising New SOI Material Technology," <u>Proceedings 1995 IEEE International SOI Conference</u> (October 1995) pp. 178-179. |
| C9 | Bruel, "Silicon on Insulator Material Technology," <u>Electronic Letters</u> , Vol. 13, No. 14 (July 6, 1995) pp. 1201-1202. |
| C10 | Bufler et al., "Hole transport in strained Si _{1-x} Ge _x alloys on Si _{1-y} Ge _y substrates," <u>Journal of Applied Physics</u> , Vol. 84, No. 10 (November 15, 1998) pp. 5597-5602. |
| C11 | Burghartz et al., "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology," <u>IEEE Transactions on Microwave Theory and Techniques</u> , Vol. 44, No. 1 (January 1996) pp. 100-104. |
| C12 | Carlin et al., "High Efficiency GaAs-on-Si Solar Cells with High Voc Using Graded GeSi Buffers," <u>IEEE</u> (2000) pp. 1006-1011 |
| C13 | Chang et al., "Selective Etching of SiGe/Si Heterostructures," <u>Journal of the Electrochemical Society</u> , No. 1 (January 1991) pp. 202-204. |
| C14 | Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 7 (July 2001) pp. 321-323. |
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| C21 | Fischetti et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," <u>J. Appl. Phys.</u> , Vol. 80, No. 4 (August 15, 1996) pp. 2234-2252. |

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- C47 König et al., "Design Rules for n-Type SiGe Hetero FETs," Solid State Electronics, Vol. 41, No. 10 (1997), pp. 1541-1547.
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- C50 Kummer et al., "Low energy plasma enhanced chemical vapor deposition," Materials Science and Engineering B89 (2002) pp. 288-295.
- C51 Kuznetsov et al., "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," J. Vac. Sci. Technol., B 13(6) (November/December 1995) pp. 2892-2896.
- C52 Langdo et al., (2002) "Preparation of Novel SiGe-free Strained Si on Insulator Substrates" IEEE International SOI Conference, pages 211-212 (XP002263057)
- C53 Larson, "Integrated Circuit Technology Options for RFIC's - Present Status and Future Directions," IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, March 1998, pp. 387-399.
- C54 Lee et al., "CMOS RF Integrated Circuits at 5 GHz and Beyond," Proceedings of the IEEE, Vol. 88, No. 10 (October 2000) pp. 1560-1571.
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- C56 Lee et al., "Strained Ge channel p-type MOSFETs fabricated on $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ virtual substrates," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A1.9.1-A1.9.5.

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- C57 Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A3.10.1-A3.10.6.
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- C59 Leitz et al., "Hole mobility enhancements in strained Si/Si_{1-y}Ge_y p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si_{1-x}Ge_x (x<y) virtual substrates," Applied Physics Letters, Vol. 79, No. 25 (December 17, 2001) pp. 4246-4248.
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- C64 Meyerson et al., "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," Applied Physics Letters, Vol. 53, No. 25 (December 19, 1988) pp. 2555-2557.
- C65 Mizuno et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS-Electron/Hole Mobility Enhancement," "2000 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, (June 13-15), IEEE New York, NY, pp. 210-211.
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10/16/07

FORM PTO - 1449

INFORMATION DISCLOSURE STATEMENT

COPY

ATTY DOCKET NO.: ASC-025DV2C1

APPLICANTS: Cheng *et al.*

SERIAL NO.: 10/802,186

FILING DATE: March 17, 2004

GROUP: Not yet assigned

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM.
INIT.

OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)

C92 Xie et al., "Semiconductor Surface Roughness: Dependence on Sign and Magnitude of Bulk Strain," The Physical Review Letters, Vol. 73, No. 22 (November 28, 1994) pp. 3006-3009.

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8-6-07

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(Based on PTO 04-07 version)

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			Application Number	10/802,186-Conf. #3869	
			Filing Date	March 17, 2004	
			First Named Inventor	Cheng	
			Art Unit	2811	
			Examiner Name	Shouxiang Hu	
Sheet	1	of	3	Attorney Docket Number	ASC-025DV2C1

U.S. PATENT DOCUMENTS					
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	A275*	US-20020167048-A1	11-14-2002	Tweet et al.	
	A276*	US-20030027381-A1	02-06-2003	Buynoski et al.	
	A277*	US-20030077867-A1	04-24-2003	Fitzgerald	
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	B50	JP-2-210816	08-22-1990		Abstract	✓
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	B53	JP-6-252046	09-09-1994		Abstract only	✓
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



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		Art Unit	2811		
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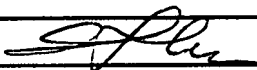
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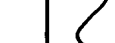
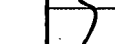
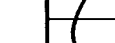
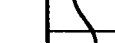


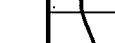
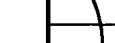



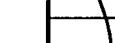





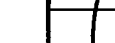

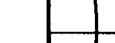


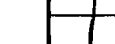
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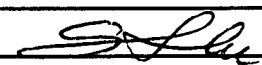
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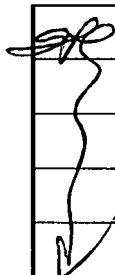
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Examiner Signature		Date Considered	10/16/07
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/802,186-Conf. #3869
				Filing Date	March 17, 2004
				First Named Inventor	Cheng
				Art Unit	2811
				Examiner Name	Shouxiang Hu
Sheet	3	of	3	Attorney Docket Number	ASC-025DV2C1

	C191	Partial International Search Report for International Patent Application No. PCT/US2006/035814, February 7, 2007 (7 pages).	
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	C193	Soderbarg, "Fabrication of BESOI-Materials Using Implanted Nitrogen as an Effective Etch Stop Barrier," 1989 IEEE SOS/SOI Technology Conference, pp. 64.	
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	C195	Wolfe et al. "Silicon Processing for the VLSI ERA, Volume 1: Process Technology," Marcel Dekker AG, New York, NY, 2000, pp. 1-35.	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.
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